## REMARKS

### Claim Rejections - 35 USC § 103

**The rejection stated:** "Claims 1-21 are rejected under 35 USC 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in combination with Houston (US Patent No. 6,261,866), Maurelli et al (US Patent No. 5,479,367) and Yamane et al (US Patent No. 6,337,249).

Applicant's admitted prior art (AAPA) discloses in figures 2 and 3 and related text a method of making a semiconductor device comprising the steps of performing a LOCOS operation on an epitaxial layer of a pre-doped N-type semiconductor substrate to define an active region have a predefined boundary (figure 3);

implanting a first dopant into the epitaxial layer within the active region to create a well of first type conductivity (figure 3, 6);

depositing a polysilicon layer over the active region, doping the polysilicon layer to create a poly semiconductor layer of a second type of conductivity, patterning the poly semiconductor layer to create a poly gate (figure 3, 1) over the first region and well;

performing an ion implant of the second type conductivity between the LOCOS regions and the poly gate to create first and second lightly doped regions (figure 3, 5 and 15), the first and second lightly doped regions being separated by a channel region beneath the poly gate;

depositing an oxide layer over the poly gate and active regions, etching the oxide layer to create side spacers (figure 3, 7 and 17) on each side of the poly gate and implanting a

heavy dose of the second type of dopant between the LOCOS regions and the side spacers to create source and drain regions (figure 3, 4 and 14), the source and drain regions being separated by the channel region. AAPA further discloses that the first type of dopant is a P type dopant and the second type of dopant is an N type dopant (Specification, p. 8 second paragraph).

AAPA fails to expressly disclose a step of implanting the first dopant into the well to create at least a first region, and also fails to teach the use of masks during the heavy dose, light dose and first region implantation steps.

Maurelli et al disclose in figures 1-3 and related text a method of implanting the first dopant into the well to create at least a first region (figure 5, 4) and discloses using a photoresist (figure 5 and 6, 3 and 5) mask during the creation of the N+ region (figure 6,9) and first region (figure 5). Maurelli further discloses implanting the N type dopant so that th lightly doped region is not in contact with the first region (figure 3). It would have been obvious to combine the teaching of Maurelli with the method of AAPA in order to guarantee a very good performance in terms of writing speed and current absorption (col. 2, lines 8-16)."

**Applicant's Response**

The AAPA and Maurelli references are not combinable because AAPA discloses making the N+ implant for the source and drain regions 4 and 14 between the side wall spacers and the LOCOS on top of the lightly doped regions 5 and 15. Whereas Maurelli

teaches implanting the source and drain regions 7 and 8 prior to implanting the lightly doped regions 16 and 17. The location of the lightly doped regions 16 and 17 is one of the key advantages to the Maurelli reference. (Please refer to column 2, lines 8 through 16.) Thus, the combination of the references is not possible without rearranging the process steps of either or both references and would not be obvious without the benefit of applicant disclosure."

**The rejection further stated:** "Neither AAPA nor Maurelli disclose implanting the N type dopant so that the lightly doped regions are in contact with the first region. Yamane et al disclose in figures 1-15D and related text a method implanting the N type dopant so that the lightly doped regions (figure 2D, 15b) are in contact with the first region (figure 2D, 17). It would have been obvious to one of ordinary skill in the art ant the time of the invention to combine the teaching of Yamane with the combined method of AAPA and Maurelli in order to establish a threshold voltage at a desired value (col. 7, lines 20-55)."

**Applicant's Response**

Yamane et al. teaches in (col. 7, lines 20-55) and in the abstract that: "A semiconductor device having an enhancement-type MOS structure which can prevent large leakage current is disclosed. A high-concentration region for threshold-value regulation use formed in a channel region below a gate electrode in an enhancement-type transistor is caused to be contiguous with a source region and not contiguous with a drain region. Herein, the distance between the high-concentration region and the drain region is set so as to preclude the

depletion layer extending from the drain region side from reaching the high-concentration region. Therefore, the electrical field in the depletion layer does not become the critical field which causes avalanche or Zener breakdown, and so leakage current can be caused to be reduced." (Emphasis added)

The emphasized limitation above is contrary to the teaching of applicant's invention and thus would not have been obvious to one of ordinary skill in the art to combine the teachings of Yamane et al. with AAPA, and Maurelli.

**The rejection further stated:** "Finally, none of the cited prior art teaches implanting the first and second region so that the two regions are separated and below the poly gate with an active region between the first and second region. Houston et at disclose in figures 1-3c a method of implanting the first and second regions so that the two regions are separated and below the poly gate with an active region between the first and second region (figures 2b and 2c). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Houston with the combined method of AAPA, Maurelli and Yamane in order to provide continued capacitive coupling of the gate of the body for a greater range of the gate voltage (col. 5, lines 30-35)."

**Applicant's Response**

Houston discloses in column 5 lines 13 through 33 that: "Referring to FIGS. 2a to 2c, there is shown an n-channel transistor in accordance with a first embodiment of the present

invention with high $V_T$ regions at the transistor sidewalls wherein **FIG. 2a is a top view and FIGS. 2b and 2c are identical cross sectional views, FIG. 2b showing the arrangement with the transistor off and FIG. 2c showing the transistor on.** As shown in FIGS. 2a to 2c, there is a moat or active region 21 which contains the same n+ source/drain regions 23 and 25 and the same P-channel region 27 as shown in FIGS. 1a and 1b. A gate electrode 29 is provided and spaced from the moat region by a gate oxide 31. A region of higher $V_T$ than for region 27, shown as a p-type region, is formed between each of the source/drain regions 23 and 25 and the channel or body region 27. A standard trench fill 32 is then provided. As can be seen in FIG. 2c, when the transistor is on, a part of the channel or body region 27 is inverted to N-type, thereby screening a portion of the body region the channel from the gate. However, in contrast to the device of FIG. 1b, the high $V_T$ regions provide continued capacitive coupling of the gate to the body for a greater range of the gate voltage." (Emphasis added)

Thus, as discussed above the identified figures show N+ source and drain regions separated by an P channel. The device is shown in one figure in the "on" state and in the other figure in the "off" and "on" conductive state.

**Applicant's Conclusion**

It is not possible to combine AAPA with Maurelli. Even if it were possible to affect such combination the teachings of Yamane and Houston would have to be substantially modified. None of which would be obvious without the benefit of applicant's disclosure.

Applicant has received an Official Action, mailed 8-22-02, to co-pending Application Serial Number: 10/026,320, filed on 12-20-01. The cited prior art is enclosed herewith on PTO form 1449. The co-pending application is based on the same specification as this application.

The specification has been amended to correct minor grammatical and or typographical errors.

The claims being in condition for allowance this action is requested.

**Respectfully submitted,**

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**Edited Paragraphs**

Page 4. Paragraph 3:
So, with the source and body grounded, the drain biased at some positive voltage (5.0 volts, for example), and the control gate biased greater than the threshold voltage (2.5 volts, for example), the NMOS transistor in an unprogrammed EPROM [is] in the "on" state and drain current flows.

Page 5. Paragraph 1:

To program the EPROM, the bias conditions are set momentarily so that there is a substantial amount of drain current flowing and hot electrons are generated. Typical bias conditions might be 7.0 volts on the drain and 12.0 volts on the control gate. With these bias conditions, a tremendous amount of hot electrons are generated in a typical 5V, 0.5 micron NMOS transistor. With 12.0 volts on the control gate, there might be 10.0 volts or more across the NMOS gate oxide according to the equation given above. This gate oxide potential "assists" the injection of hot electrons (which already have an abundance of energy) through the gate oxide onto the polysilicon gate. Since the polysilicon gate is a floating gate without connections, these electrons are trapped here due to the oxide insulators which encapsulate the polysilicon once the programming event is completed. After ~200 milliseconds (a typical duration of the programming event), the amount of electrons trapped on the floating gate is significant and sufficient to drastically impact the NMOS transistor characteristics. During such programming, it is possible to increase the NMOS transistor threshold voltage to 4.0-10.0 volts. Assuming this new, higher threshold voltage and the same operating bias conditions described above (5.0 volts on the drain and 2.5 volts on the control gate), the NMOS transistor of the EPROM is now in the "off" state (negligible drain current flowing). By selectively programming EPROMs on a circuit depending on the circuit behavior, the circuit can be trimmed or fine-tuned to enhance its performance. It should be noted at this time that 200 milliseconds to program a single EPROM can be very costly. On a complex circuit, it is possible that several programming iterations must be performed for each circuit

which can significantly added to the probe/test cost. A faster programming EPROM could reduce probe/test cost significantly.

Page 9, Paragraph 2:

Referring to Figure 4, there is illustrated a top down view of an NMOS transistor 101 suitable for use as an EPROM cell according to the invention. The NMOS transistor 101 includes a drain 2 and a source 3 of a $N^+$ regions 4 and 14. Additionally, there is a poly gate 1 with a P well 6 located beneath the poly gate 1 and the $N^+$ regions 4 and 14. Lightly doped drain (Nldd) regions 5 and 15 are located beneath the $N^+$ regions 4 and 14 and extends into the channel region under the poly gate 1. Oxide spacers 7 and 17 are located on the top surface of the substrate adjacent to the poly gate 1 and [is] are used during the implanting of the $N^+$ region 4 and 14 as a masked for the drain 2 and source 3. Novel P regions 8 and 18 are located beneath the poly gate 1 and separated from the $N^+$ regions 4 and 14 by the Nldd regions 5 and 15, respectively. The P regions 8 and 18 extend into the P well 6 from the outer periphery 51 but are not present in the center 50 of the NMOS transistor 101. In a pure CMOS process flow, the new P regions 8 and 18 and the P well 6 are positioned prior to the poly gate 1 formation.

Page 9, Paragraph 3:

The P regions 8 and 18 may or may not be completely counter dope to the Nldd region 5 and 15 and may or may not actually intersect with the $N^+$ regions 4 and 14. The purpose of the P regions 8 and 18 [are] is to increase the electric field between the $N^+$ region 4 and P well 6. This increase in the electric field will increase the hot electron generation rate in programming an EPROM cell and thus will enable the NMOS transistor 101 to be programmed quicker and possibly at a lower voltage than the prior art devices.